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<u>S13239</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(writeback or (write adj back)) and (cache adj tag) and (morrow-michael\$.in.)	2007-05-04 14:31:52	
<u>S13238</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	morrow-michael\$.in.	2007-05-04 14:31:42	
<u>S13237</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	tag with (writeback or (write adj back) near2 bit)	2007-05-04 14:17:58	
<u>S13236</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(cache adj tag) with (writeback or (write adj back) near2 bit)	2007-05-04 14:15:08	
<u>S13235</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(writeback or (write adj back)) near2 (bit)	2007-05-04 14:11:52	
<u>S13234</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	bit	2007-05-04 14:11:27	
<u>S13233</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	writeback or (write adj back)	2007-05-04 14:00:18	
<u>S13232</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	cache adj tag	2007-05-04	

			13:59:33
<u>S13231</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD 6327643.pn.	2007-05-04 10:13:38
<u>S13230</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD 6134634.pn.	2007-05-04 09:47:36
<u>S13229</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD 6134634.pn.	2007-05-04 08:48:55
<u>S13228</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD (writeback or (write adj back) near3 tag or status) and (711/(143-145).ccls.)	2007-05-03 17:57:36
<u>S13227</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD 711/(143-145).ccls.	2007-05-03 17:57:27
<u>S13226</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD (writeback or (write adj back)) near3 (tag or status)	2007-05-03 17:56:17
<u>S13225</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD tag or status	2007-05-03 17:55:50
<u>S13224</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD writeback or (write adj back)	



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IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 1. Architecture and circuit techniques for a 1.1-GHz 16-kb reconfigurable memory in 0.18- μm CMOS
 Mai, K.; Ho, R.; Alon, E.; Liu, D.; Younggon Kim; Patil, D.; Horowitz, M.A.;
Solid-State Circuits, IEEE Journal of
 Volume 40, Issue 1, Jan. 2005 Page(s):261 - 275
 Digital Object Identifier 10.1109/JSSC.2004.837992
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IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

- ☐ 1. **An area model for on-chip memories and its application**
Mulder, J.M.; Quach, N.T.; Flynn, M.J.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 26, Issue 2, Feb. 1991 Page(s):98 - 106
Digital Object Identifier 10.1109/4.68123
[AbstractPlus](#) | [Full Text: PDF\(760 KB\)](#) IEEE JNL
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- ☐ 2. **Tag compression for low power in dynamically customizable embedded processors**
Petrov, P.; Orailoglu, A.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
Volume 23, Issue 7, July 2004 Page(s):1031 - 1047
Digital Object Identifier 10.1109/TCAD.2004.829823
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(560 KB\)](#) IEEE JNL
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- ☐ 3. **Architecture and circuit techniques for a 1.1-GHz 16-kb reconfigurable memory in 0.18- μ m CMOS**
Mai, K.; Ho, R.; Alon, E.; Liu, D.; Younggon Kim; Patil, D.; Horowitz, M.A.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 40, Issue 1, Jan. 2005 Page(s):261 - 275
Digital Object Identifier 10.1109/JSSC.2004.837992
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- ☐ 4. **Design and implementation of an embedded 512-KB level-2 cache subsystem**
Shin, J.L.; Petrick, B.; Singh, M.; Leon, A.S.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 40, Issue 9, Sept. 2005 Page(s):1815 - 1820
Digital Object Identifier 10.1109/JSSC.2005.852165
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- ☐ 5. **High-throughput, low-memory applications on the Pica architecture**
Wills, D.S.; Cat, H.H.; Cruz-Rivera, J.; Lacy, W.S.; Baker, J.M., Jr.; Eble, J.C.; Lopez-Lagunas, A.; Hopper, M.;
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- ☐ 6. **A 450-MHz RISC microprocessor with enhanced instruction set and copper interconnect**
Nicoletta, C.; Alvarez, J.; Barkin, E.; Chai-Chin Chao; Johnson, B.R.; Lassandro, F.M.; Patel, P.; Reid, D.; Sanchez, H.; Seigel, J.; Snyder, M.; Sullivan, S.; Taylor, S.A.; Minh Vo;
[Solid-State Circuits, IEEE Journal of](#)
Volume 34, Issue 11, Nov. 1999 Page(s):1478 - 1491
Digital Object Identifier 10.1109/4.799852
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(824 KB\)](#) IEEE JNL
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- ☐ 7. **A CAM with mixed serial-parallel comparison for use in low energy caches**
Efthymiou, A.; Garside, J.D.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 12, Issue 3, March 2004 Page(s):325 - 329
Digital Object Identifier 10.1109/TVLSI.2004.824298
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(248 KB\)](#) IEEE JNL
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